REMARKS

After entry of this amendment, claims 1, 3, 9-13, 15, and 21-29 are pending. Support for the amendments made in this response can be found throughout the present specification. See, e.g., Fig. 9 and the corresponding description thereof. In the present Office Action, claims 1, 3-11, 13, 15-21, 23-24, and 29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Wang, U.S. Patent No. 5,956,746 ("Wang"). Claims 25-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Tran, U.S. Patent No. 6,115,792 ("Tran"). Claims 12 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Wickeraad et al., U.S. Patent No. 6,490,654 ("Wickeraad"). Applicants respectfully traverse these rejections and request reconsideration.

Art Rejection

Applicants respectfully submit that claims 1, 3, 9-13, 15, and 21-29 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "there is a one-to-one correspondence between the different corresponding cache lines and the plurality of values, and the plurality of bits forming a given value of the plurality of values, as a whole, is the value associated with the different cache line, and wherein each bit of the plurality of bits of the given value is formed from a logical combination of two or more virtual address bits from a virtual address that corresponds to the different cache line; a way prediction generator circuit coupled to receive a first virtual address corresponding to the first address, and wherein the way prediction generator logically combines bits of the first virtual address to generate a first value during use; and a circuit coupled to receive the plurality of values and the first value and the first value comprising a second plurality of bits, wherein the circuit compares the first value to the plurality of values during use, and wherein a match of the first value and a second value stored in a first way of the plurality of ways causes the circuit to predict the first way to be a hit in the cache for the first address for the current access during use."

Wang, on the other hand, compares subsets of the address bits to make a way

prediction: "A particular set in predictor tag array 80 is identified by the set information bits (bits 5-15) of the address through conductor 66 to read/write circuitry 92. Set 84 is one of the 2K sets. Set 84 includes four four-bit tag way information numbers 84-0, 84-1, 84-2, and 84-3, associated with way 0 (W0), way 1 (W1), way 2 (W2), and way 3 (W3), respectively. Each of the four address way information numbers 84-0, 84-1, 84-2, and 84-3 is a four-bit number. That is the same number of bits that are included in the address tag way bits (bits 16-19) of address register 64. When a particular set is selected by bits 5-15, the way information numbers 84-0, 84-1, 84-2, and 84-3 are provided through conductors 88-0, 88-1, 88-2, and 88-3 to comparator circuitry 94 and compared with address tag way bits (bits 16-19) of the address of address register 64. For example, assuming set 84 is selected by bits 5-15, the four four-bit numbers 84-0, 84-1, 84-2, and 84-3 are compared in comparator circuitry 94 with bits 16-19. If none of the four four-bit numbers 84-0, 84-1, 84-2, and 84-3 match bits 16-19, then there is a cache miss and processor 52 looks elsewhere for the data of interest. If only one of the four four-bit numbers match bits 16-19, then a way prediction signal (e.g., 2 bits) is provided on conductors 62 to cache controller 58 to represent the predicted way that is associated with the tag way information number matched." See Wang, col. 3, line 58-col. 4, line 15. Thus, a subset of the address bits from each tag (read from the predictor tag array) is simply compared to the corresponding address bits of the address accessing the cache (stored in the address register). This does not teach or suggest "each bit of the plurality of bits of the given value is formed from a logical combination of two or more virtual address bits from a virtual address that corresponds to the different cache line; … the way prediction generator logically combines bits of the first virtual address to generate a first value" as recited in claim 1.

With regard to claims 7 and 8, the Office Action asserts that "any bit could be considered a logical combination of two other bits if the logical combination is not defined." However, Applicants note that the features of claim 1 recite "each bit of the plurality of bits of the given value is formed from a logical combination of two or more virtual address bits from a virtual address that corresponds to the different cache line." In order to anticipate such a limitation, Wang would have to teach the logical combination

of virtual address bits to form a value for comparison. Wang teaches no such combination, and thus does not teach or suggest the above highlighted features.

Furthermore, claim 1 recites comparing logical combinations of virtual address bits. Wang only teaches the use of physical address bits. See, e.g., Wang, col 3, lines 15-18. Accordingly, Wang does not anticipate claim 1 for at least this additional reason.

For at least all of the above reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 13 and 23 each recite combinations of features including features similar to those highlighted above. Accordingly, claims 13 and 23 are patentable over the cited art. Claims 3, 9-12, 15, 21-22, and 24-29 depend from one of claims 1, 13, or 23 and recite additional combinations of features not taught or suggested in the cited art.

Claim Objection

Claims 1, 13, and 23 were objected to, and the Examiner noted a typographical error. Applicants have corrected the error, and respectfully submit that the objection is addressed.

Examiner Invitation

If the Examiner have any questions or suggestions regarding the present amendment and response, the Examiner is invited to contact the undersigned for discussion.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested. If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/6363-00600/LJM.

Respectfully submitted,

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